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SUITE 3100
PITTSBURGH, PA 15219-2502

EXAMINER	
TRAN, MICHAEL THANH	
ART UNIT	**PAPER NUMBER**
2827	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/899,977	KEETH ET AL.	
	Examiner	Art Unit	
	MICHAEL T. TRAN	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *70,71,100,120,135,136,143,147,152,160-165,167-188 and 196-208* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *70,71,100,120,135,136,143,147,152,160-165,167-188 and 196-208* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

MICHAEL TRAN
AU 2827

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/23/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In response to the Communications dated May 17, 2007, claims 70, 71, 100, 120, 135, 136, 143, 147, 152, 160-165, 167-188 and 196-208 are active in this application as a result of the cancellation of claims 1-69, 72-99, 101-119, 121-134, 137-142, 144-146, 148-151, 153-159, 166 and 189-195.

Information Disclosure Statement

2. The information disclosure statements filed August 23, 2004 have been considered.

Claim Objections

3. It appears that claim 199 is unclear when it recites, "step of inputting at least one address includes the step of inputting a first address for confirming that the device is to be in a test mode and inputting a second address for specifying a test mode". Should the limitation of "at least one address" be changed to "at least two addresses", since it contains two addresses – a first address and a second address. As for now, the interpretation for this recitation will be in regard to just one of the two specified.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated

by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 70 and 167-173 are rejected on the ground of nonstatutory obviousness type double patenting as being unpatentable over claims 1-67 of U.S. Patent No. 6,324,088 ['088]. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reasons.

Similar to the claimed invention, claim 1 of the patent '088 recites "...an array of memory cells...a plurality of peripheral devices for writing data...reading data...a plurality of voltage supplies...test mode logic..." Unlike the claimed invention, claim 1 of the patent '088 further describes that the cells contain two elements. However, one of ordinary skilled in the art would recognize that dram cells normally have two elements – a transistor and a capacitor. Therefore, it is evident that coverage has already been given to the claimed limitations. Further, it has been held that omission of an element and its function in a combination where the remaining elements perform the same functions as before involves only routine skill in the art. In re Karlson, 136 USPQ 184.

For similar reasons indicated above, claims 167-173 are unpatentable over claims 1-67 of patent '088.

5. Claims 71, 174 and 175 are rejected on the ground of nonstatutory obviousness type double patenting as being unpatentable over claims 1-67 of U.S. Patent No. 6,324,088 ['088]. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reasons.

Similar to the claimed invention, claim 51 of the patent '088 recites, "...writing test data...latching the test data...comparing the test data..." Unlike the claimed invention, claim 51 of the patent '088 does not include the term "seed" to further limits the term row of a memory. However, one of ordinary skill in the art would recognize that they are one in the same. Therefore, it is evident that coverage has already been given to the claimed limitations.

For similar reasons indicated above, claims 174 and 175 are unpatentable over claims 1-67 of patent '088.

6. Claims 100 and 176-186 are rejected on the ground of nonstatutory obviousness type double patenting as being unpatentable over claims 1-67 of U.S. Patent No. 6,324,088 ['088]. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reasons.

Similar to the claimed invention, claim 20 of the patent '088 recites, "...a control unit for performing a series...a plurality of peripheral devices...a plurality of voltage

supplies...test mode logic..." Unlike the claimed invention, claim 20 of the patent '088 does not include the term "seed" to further limits the term row of a memory. However, one of ordinary skill in the art would recognize that they are one in the same. Therefore, it is evident that coverage has already been given to the claimed limitations.

For similar reasons indicated above, claims 176-186 are unpatentable over claims 1-67 of patent '088.

7. Claims 120, 187 and 188 are rejected on the ground of nonstatutory obviousness type double patenting as being unpatentable over claims 1-67 of U.S. Patent No. 6,324,088 ['088]. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reasons.

Similar to the claimed invention, claim 41 of the patent '088 recites, "...test mode logic...a latching circuit...enable circuit..." Unlike the claimed invention, claim 41 of the patent '088 further recites that the enable circuit is a write enable circuit. However, one of ordinary skill in the art would recognize they are functionally equivalent. Therefore, it is evident that coverage has already been given to the claimed limitations.

For similar reasons indicated above, claims 187 and 188 are unpatentable over claims 1-67 of patent '088.

8. Claims 135 and 136 are rejected on the ground of nonstatutory obviousness

type double patenting as being unpatentable over claims 1-67 of U.S. Patent No. 6,324,088 ['088]. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reasons.

Similar to the claimed invention, claim 52 of the patent '088 recites, "...selecting a memory block...writing test data...latching test data...comparing the test data..." Unlike the claimed invention, claim 52 of the patent '088 does not include the term "seed" to further limits the term row of a memory. However, one of ordinary skill in the art would recognize that they are one in the same. Therefore, it is evident that coverage has already been given to the claimed limitations.

For similar reasons indicated above, claim 136 is unpatentable over claims 1-67 of patent '088.

9. Claims 143 and 196-199 are rejected on the ground of nonstatutory obviousness type double patenting as being unpatentable over claims 1-67 of U.S. Patent No. 6,324,088 ['088]. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reasons.

Similar to the claimed invention, claim 55 of the patent '088 recites, "...inputting to the device...enabling...confirming..." Unlike the claimed invention, claim 55 of the patent '088 further includes a step of inhibiting. However, one of ordinary skill in the art would recognize the two methods, overall, are similar to each other. Therefore, it is evident that coverage has already been given to the claimed limitations.

For similar reasons indicated above, claims 196-199 are unpatentable over claims 1-67 of patent '088.

10. Claims 147 and 200-202 are rejected on the ground of nonstatutory obviousness type double patenting as being unpatentable over claims 1-67 of U.S. Patent No. 6,324,088 ['088]. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reasons.

Similar to the claimed invention, claim 56 of the patent '088 recites, "...applying...inputting at least two addresses...confirm..." Unlike the claimed invention, claim 56 of the patent '088 further includes the recitation of sequentially inputting at least two addresses. However, one of ordinary skill in the art would recognize the two methods, overall, are similar to each other. Therefore, it is evident that coverage has already been given to the claimed limitations. Further, it has been held that the provision of adjustability, where needed, involves only routine skill in the art. In re Stevens, 101 USPQ 284 [CCPA 1954].

For similar reasons indicated above, claims 200-202 are unpatentable over claims 1-67 of patent '088.

11. Claims 152 and 203-208 are rejected on the ground of nonstatutory obviousness type double patenting as being unpatentable over claims 1-67 of U.S. Patent No. 6,324,088 ['088]. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reasons.

Similar to the claimed invention, claim 60 of the patent '088 recites, "...applying verifying..decoding..." Unlike the claimed invention, claim 60 of the patent '088 further includes the application of a write control signal along with a column address strobe. However, one of ordinary skill in the art would recognize the two methods, overall, are similar to each other. Therefore, it is evident that coverage has already been given to the claimed limitations. Further, it has been held that the provision of adjustability, where needed, involves only routine skill in the art. In re Stevens, 101 USPQ 284 [CCPA 1954].

For similar reasons indicated above, claims 203-208 are unpatentable over claims 1-67 of patent '088.

12. Claims 160, 161 and 162 are rejected on the ground of nonstatutory obviousness type double patenting as being unpatentable over claims 1-67 of U.S. Patent No. 6,324,088 ['088]. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reasons.

Similar to the claimed invention, claim 67 of the patent '088 recites, "...a test logic circuit...a test mode enable circuit...a circuit for receiving and decoding..." Unlike the claimed invention, claim 67 of the patent '088 further includes the application of a write control signal along with a column address strobe. However, the basic structures are the same. Therefore, it is evident that coverage has already been given to the claimed limitations. Further, it has been held that the provision of adjustability, where

needed, involves only routine skill in the art. In re Stevens, 101 USPQ 284 [CCPA 1954].

For similar reasons indicated above, claims 161 and 162 are unpatentable over claims 1-67 of patent '088.

13. Claims 163, 164 and 165 are rejected on the ground of nonstatutory obviousness type double patenting as being unpatentable over claims 1-67 of U.S. Patent No. 6,324,088 ['088]. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reasons.

Similar to the claimed invention, claim 67 of the patent '088 recites, "...a test logic circuit...a test mode enable circuit...a circuit for receiving and decoding..." Unlike the claimed invention, claim 67 of the patent '088 further includes the application of a write control signal along with a column address strobe. However, the basic structures are the same. Therefore, it is evident that coverage has already been given to the claimed limitations. Further, it has been held that the provision of adjustability, where needed, involves only routine skill in the art. In re Stevens, 101 USPQ 284 [CCPA 1954].

For similar reasons indicated above, claims 164 and 165 are unpatentable over claims 1-67 of patent '088.

14. Claims 70, 71, 100, 120, 135, 136, 167-172, and 174-188 are provisionally

rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-7 of copending Application No. 20070008811 ['811]. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reasons.

Similar to the claimed invention, the claims in Application '811 recites a general concept of writing data to one memory, latch the data from that memory then transfer it to a secondary memory, in response to external signals. Unlike the claimed invention, Application '811 does not specifically recites the particular circuitry that will perform the above steps. However, one of ordinary skill in the art would recognize that the steps recited in the claims and the steps recited in the Application are similar. Therefore, coverage for the invention has already been given. It is noted that it has been held that omission of an element and its function in a combination where the remaining elements perform the same functions as before involves only routine skill in the art. In re Karlson, 136 USPQ 184.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections- 35 U.S.C. § 102

15. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in-
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

16. Claims 143 and 196-199 are rejected under 35 U.S.C 102(b) as being anticipated by Keeth [U.S. Patent # 5,651,011].

With respect to claim 143, Keeth disclose, in figures 1 and 2, a method of inputting test mode information to a solid state device, comprising: enabling a detector [via 34]; inputting to the device a voltage outside the range of voltages used to represent logic signals [super voltage via 32]; confirming the presence of the voltage outside the range of voltages used to represent logic signals [via 40 and 12]; and inputting to the device at least one address containing test mode information [via 36]. It is noted that it has been held that omission of an element and its function in a combination where the remaining elements perform the same functions as before involves only routine skill in the art. In re Karlson, 136 USPQ 184. Additionally, it has also been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

With respect to claim 196, Keeth disclose, in figures 1 and 2, said step of enabling a detector is performed by the step of inputting a sequence of control signals. See figure 2 – ras, cas, we.

With respect to claim 197, Keeth disclose, in figures 1 and 2, said sequence of control signals includes a write enable signal [WE], column address strobe signal [CAS] and row address strobe signal [RAS].

With respect to claim 198, Keeth disclose, in figures 1 and 2, said step of inputting at least one address to the device is performed while said step of inputting a voltage is performed. See figure 1.

With respect to claim 199, Keeth disclose, in figures 1 and 2, said step of inputting at least one address includes the step of inputting a first address for confirming that the device is to be in a test mode and inputting a second address for specifying a test mode – via 70 or 36.

17. Claims 147 and 200-202 are rejected under 35 U.S.C 102(b) as being anticipated by Keeth [U.S. Patent # 5,651,011].

With respect to claim 147, Keeth disclose, in figures 1 and 2, a method of placing a solid state device into a test mode, comprising: applying to the device a voltage [via 32] outside the range of voltages used to represent logic signals, and while said voltage is being applied; sequentially inputting at least two addresses to said device, said first address containing information used to confirm the presence of said voltage outside the range of voltages used to represent logic signals, and said second address containing

information used to place the device into a test mode [Keeth indicated that there are two elements within a test mode – first, a test mode address vector; and second, a corresponding particular test mode]. It is noted that it has been held that omission of an element and its function in a combination where the remaining elements perform the same functions as before involves only routine skill in the art. In re Karlson, 136 USPQ 184. Additionally, it has also been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

With respect to claim 200, Keeth disclose additionally comprising the step of inhibiting the device from normal operation while said step of applying a voltage is performed. See figure 4 and entire document, especially, the "Detailed Description" section. Keeth indicated that there exists a lockout state latch functioning to inhibit certain test operation.

With respect to claim 201, Keeth disclose additionally comprising the step of ending the application of a voltage outside the range of voltages used to represent logic signals to take the device out of a test mode. See figure 4 and entire document, especially, the "Detailed Description" section.

With respect to claim 202, Keeth disclose additionally comprising the step of inputting an address containing information to take the device out of a test mode. See figure 4 and entire document, especially, the "Detailed Description" section.

18. Claims 160-162 are rejected under 35 U.S.C 102(b) as being anticipated by

Keeth [U.S. Patent # 5,651,011].

With respect to claim 160, Keeth disclose a test logic circuit for a solid state memory device, comprising: a test mode enable circuit [22] for determining if a voltage outside the range of voltages used to represent logic levels is being applied to the memory device under predetermined conditions; and a circuit for receiving and decoding test mode keys [12] in response to said test mode enable circuit. It is noted that it has been held that omission of an element and its function in a combination where the remaining elements perform the same functions as before involves only routine skill in the art. In re Karlson, 136 USPQ 184. Additionally, it has also been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

With respect to claim 161, Keeth disclose additionally comprising a test mode reset circuit for resetting said circuit for receiving and decoding test mode keys. See entire document, especially, the "Detailed Description" section.

With respect to claim 162, Keeth disclose additionally comprising a circuit [24] for inhibiting said solid state memory device from normal operations when the device is in a test mode. Also see figure 4 and the entire document, especially, the "Detailed Description" section. It is noted that it has been held that omission of an element and its function in a combination where the remaining elements perform the same functions as before involves only routine skill in the art. In re Karlson, 136 USPQ 184.

19. Claims 163-165 are rejected under 35 U.S.C 102(b) as being anticipated by

Keeth [U.S. Patent # 5,651,011].

With respect to claim 163, Keeth disclose, in figures 1 and 2, A solid state memory device, comprising: a plurality of memory cells [within 52]; a plurality of peripheral devices for writing information into and reading information out of said memory cells [64 and 66]; and a test logic circuit [54], comprising: a test mode enable circuit [22] for determining if a voltage outside the range of voltages used to represent logic levels is being applied to the memory device under predetermined conditions; and a circuit [36] for receiving and decoding test mode keys in response to said test mode enable circuit; said memory device further comprising circuits [12], responsive to said decoded test mode keys, for performing tests on at least one of said memory cells and peripheral devices. See entire document. It is noted that it has been held that omission of an element and its function in a combination where the remaining elements perform the same functions as before involves only routine skill in the art. In re Karlson, 136 USPQ 184. Additionally, it has also been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

With respect to claim 164, Keeth disclose, said test mode enable circuit includes logic for receiving a row address strobe signal (RAS), a write column address strobe before RAS signal, the applied voltage, and certain address information on column address lines and for producing therefrom a latch signal. See figure 2.

With respect to claim 165, Keeth disclose, additionally comprising a test mode reset circuit for resetting said circuit for receiving and decoding test mode keys – 70. See entire document.

Conclusion

20. When responding to the Office action, Applicants are advised to provide the Examiner with line and page numbers of the application and/or references cited to assist the Examiner in the prosecution of this case.

21. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Michael T. Tran whose telephone number is (571) 272-1795. The Examiner can normally be reached on Monday-Thursday from 7:30-6:00 P.M.

22. Any inquiry of a general nature or relating to the status of this application. should be directed to the Group receptionist whose telephone number is (571) 272-1650.

Michael T. Tran
Art Unit 2827
June 15, 2007